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Active Autonomous Open-Loop Technique for Static and Dynamic Current Balancing of Parallel-Connected Silicon Carbide MOSFETs

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Abstract: Silicon carbide (SiC) MOSFETs tend to become one of the main switching elements in power electronics applications of medium- and high-power density. Usually, SiC MOSFETs are connected in parallel to increase power rating. Unfortunately, unequal current sharing between power devices occurs due to mismatches in the technical parameters between devices and the layout of the power circuit. This current imbalance causes different current stress upon power switches, raising concerns about power system reliability. For over a decade, various methods and techniques have been proposed for balancing the currents between parallel-connected SiC MOSFETs. However, most of these methods cannot be implemented unless the deviation between the technical parameters of semiconductor switches is known. This requirement increases the system cost because screening methods are extremely costly and time-consuming. In addition, most techniques aim at suppressing only the transient current imbalance. In this paper, a simple but innovative current balancing technique is proposed, without the need of screening any power device. The proposed technique consists of an open-loop system capable of balancing the currents between two parallel-connected SiC MOSFETs, with the aid of two active gate drivers and an FPGA, actively and independently of the cause. Experimental test results validate that the proposed open-loop method can successfully achieve suppression of current imbalance between parallel-connected SiC MOSFETs, proving its durability and validity level.

Keywords: energy systems; energy system components; parallel-connected silicon carbide (SiC) MOSFETs; active current balancing technique; optimization models

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1. Introduction

Power electronic systems and applications are considered to be one of the most essential parts of renewable energy sources (RES), electric vehicles (EV), EV chargers, and EV main inverters, reducing the environmental impact. High-capacity, high-temperature, and high-frequency power converters are increasingly demanded to increase power density, reduce costs, and save manpower. For this reason, the most significant features of new technology power converters are minimization of volume, maximization of efficiency, high reliability, and increased durability against short-circuit/overvoltage conditions. To achieve these goals, the transaction from silicon (Si) to wide band gap (WBG)-based semiconductor power switches is of great significance because of their outstanding features compared to Si ones.

Among WBG power switches, SiC MOSFET is considered to be the most promising alternative solution to conventional semiconductor devices in medium- and high-power-density power converter fields. This is attributed to its exceptional characteristics, such as the relatively mature technology, the low cost, and its more stable construction [1,2]. Indeed, the most significant features of SiC MOSFET are the high thermal conductivity and

operating temperature capability, the higher breakdown voltage, its superior switching characteristics, the lower on-resistance, the usage of low complexity gate drivers, and the normally-off characteristic. Moreover, SiC MOSFET has no tail current leading to reduced switching losses as well as higher switching frequency [1–3].

Nevertheless, SiC MOSFET offers less current capability than Si ones due to its smaller chip area. This derives from the lower maturity of the manufacturing process of SiC MOSFETs compared to Si ones which includes the lower yield in the wafer as well as the high thermal and mechanical stress in the device. As a result, the current ratings of commercially available discrete SiC MOSFETs with a maximum blocking voltage of 1.2 kV and 1.7 kV are within 120 A and 100 A, respectively. For this reason, the current rating is usually boosted by connecting multiple SiC MOSFET devices in parallel [4–8].

However, the parallelization of SiC MOSFETs introduces the problem of current imbalance which is unpredictable. This results in uneven conduction and switching losses between parallel devices. This, in turn, causes uneven sharing of junction temperature, increasing the risk of SiC MOSFET(s) being led to thermal runaway [9,10]. Also, an overcurrent and, at the same time, overheating is quite possible. Therefore, it is essential to overcome any possibility of power device failure due to high junction temperature swing by suppressing the current imbalance and retaining distributed heat between power devices as equally as possible [4,11,12].

Current imbalance can be caused by a device package parameter mismatch. For instance, the variation in on-state resistance ($R_{DS\text{-}on}$) causes unequal current sharing during the steady-state, leading to static current imbalance. Moreover, any difference in threshold voltage (V_{th}) and trans-conductance (g_m) leads to uneven current distribution during turn-on and -off intervals, causing dynamic current imbalance [4]. Puschkarsky et al., in [13], experimentally proved the V_{th} instability of high-voltage SiC MOSFETs which may be either short-time or even permanent. Asymmetry of the PCB layout of the power circuit may also affect the current sharing of power devices [14]. Also, both types of imbalances result in unequal temperature rises and electromagnetic interference (EMI), endangering system reliability.

Over the last decade, the current imbalance issue has been addressed by many researchers, proposing techniques and methods capable of minimizing one or both current imbalance types between discrete parallel-connected SiC MOSFETs.

Refs. [4,15,16] proposed several active current balancing methods that make use of current sensors to actively detect current imbalance. Subsequently, an analog controller receives the dynamic imbalance and suppresses it through a gate driver by matching the switching behaviors of the parallel switches.

Most proposed methods suppress static or/and dynamic current imbalance by using passive elements. Refs. [11,17] mitigated dynamic imbalance by adding extra coupled inductance and external same-size gate resistors. As a result, control voltages of parallel devices vary only during transient stages, eliminating the entire transient imbalance. In the same way, ref. [18] eliminated dynamic imbalance with the addition of different-size gate resistors differentiating each gate loop impedance and eliminating turn-on dynamic imbalance. Ref. [19] also deals with turn-on dynamic imbalance by making the gate resistor of the power switch with the smallest V_{th} greater, delaying the charging process of its input capacitance (C_{iss}). In refs. [8,20], static current imbalance was suppressed by adding same-size resistors, serially connected with the drains of the parallel-connected devices. In addition, ref. [8] mitigates both types of imbalances with a differential mode choke. Similarly, refs. [21,22] suppressed the overall current imbalance with the incorporation of a series-connected coupled inductor with the drains of power devices. On the other hand, ref. [23] suggests an alternative way to implement the two aforementioned methods to suppress current imbalance and avoid the disadvantages provoked by the usage of a coupled inductor. Finally, ref. [24] eliminates the entire imbalance by connecting a planar transformer in series with the drains of each power device.

Refs. [1,25–30] proposed novel screening methods for discovering SiC MOSFETs with very close technical parameters, such as $R_{DS\text{-}on}$, V_{th}, and g_m, achieving a balanced current distribution without the requirement of a current imbalance suppression technique. Based on [10,31], the current imbalance, caused by the asymmetrical PCB layout of the power circuit, can be mitigated by lowering the deviations between drain and common source parasitic inductances. Nonetheless, ref. [32] deals with the imbalance, attributed to the asymmetry of the power circuit layout by incorporating a common mode choke to each parallel SiC MOSFET gate loop. This method holds that the current imbalance is limited as the choke mutual inductance becomes larger. Ref. [33] achieved an optimal transient current sharing by reducing the gate resistance, weakening the effect of V_{th} mismatch.

In addition, ref. [34] proposes a gate driver that generates PWMs with different time delays of picoseconds, suppressing dynamic imbalance. Additionally, ref. [35] balances the dynamic imbalance with a multi-stage gate driver with the ability to change the gate resistor during the transient stages. Finally, ref. [36] proposes a gate driver capable of varying the gate voltage to mitigate transient current imbalance.

All the aforementioned methods have the ability to eliminate either static or/and dynamic current imbalance between parallel SiC MOSFETs. On the other hand, most techniques cannot be implemented unless the technical parameters of SiC MOSFETs are known. For this reason, screening processes are needed and conducted with the aid of power device analyzers/curve tracers [20]. Also, ref. [37] proposed a method to monitor the on-resistance of SiC MOSFET. This necessity can be an inhibiting factor for their application in the industry since screening is an extremely costly and time-consuming process [4]. The implementation of the methods, proposed by refs. [4,15,16], can be realized without any screening process since dynamic current imbalance is mitigated with a closed-loop method that actively monitors and suppresses transient imbalance. However, static current imbalance suppression is not addressed. As a result, none of these techniques can minimize the whole current imbalance without knowledge of the device parameter mismatch. Also, the validity of most methods has not been tested under the condition of an asymmetrical PCB layout.

In this paper, an innovative, active, and autonomous open-loop current balancing technique is proposed which addresses the imbalance issue without the necessity of knowing the technical parameters of the power devices. In addition, the proposed technique can eliminate static and dynamic current imbalances actively and irrelevantly of the cause. In Section 2, an analysis to investigate potential strategies for current imbalance suppression is conducted. In Section 3, an analytical description of the structure, functions, and design guidelines of the active current balancing technique is provided. In Section 4, two experimental tests are conducted to verify its effectiveness and efficiency. In Section 5, extension guidelines of the proposed current balancing technique are proposed. Finally, in Section 6, the most important conclusions of this research are presented.

2. Strategies of Static and Dynamic Current Balancing

In this section, an analysis concerning the factors that lead to static and dynamic imbalance is conducted. In addition, an investigation to suppress both current imbalance types between parallel SiC MOSFETs is performed.

2.1. Strategies of Dynamic Current Imbalance Suppresion

As pointed out earlier, device parameter mismatch and parasitic element deviation of the power circuit cause dynamic current imbalance. Based on Equation (1), the technical parameters of the device affect its turn-on delay ($t_{d(on)}$). In this way, during turn-on transience, device parameter mismatch results in different $t_{d(on)}$ between parallel power devices leading to transient current imbalance [16].

$$t_{d(on)} = C_{iss} R_G \, ln\left(\frac{V_{CC}}{V_{CC} - V_{th}}\right) \quad (1)$$

In addition, during turn-on transience and before the drain–source voltage (V_{DS}) begins to fall, the power switch current becomes maximal [16]. At this stage, the power switch is in saturation mode and its current is expressed by Equation (2).

$$\frac{di_D}{dt} = \frac{V_{CC} - V_{th} - i_D/g_m}{L_S + R_G C_{iss}/g_m} \tag{2}$$

i_D is the drain current; V_{CC} is the activating voltage of SiC MOSFET; L_S is the source parasitic inductance of the gate and power loop; di_D/dt is the slew rate of drain current; and R_G is the gate resistance. According to Equation (2), the drain current slew rate is dependent on several factors. Therefore, any deviation of these parameters between parallel-connected SiC MOSFETs can affect transient current sharing causing dynamic current imbalance. Equations (1) and (2) can be similarly written for the turn-off transition.

Based on Equations (1) and (2), the magnitude of R_G affects t_d and di_D/dt [16]. The equivalent circuit of two power devices (dashed line) along with their gate drivers, during transient stages, is depicted in Figure 1. According to Figure 1, each time the SiC MOSFET drivers output V_{CC}, the gate-drain and gate-source capacitances of the two parallel MOSFETs ($C_{GD,i}$ and $C_{GS,i}$, respectively) begin to charge by gate current ($i_{G,i}$) which is expressed in Equation (3). In the preceding symbols and below, wherever an index i appears it refers to a parameter and quantity of MOSFET 1 when $i = 1$ and MOSFET 2 when $i = 2$. Also, $C_{DS,i}$ is the drain–source capacitance of the power device. As shown in Figure 1, $i_{GD,i}$, $i_{GS,i}$, and $i_{DS,i}$ are the currents that conduct $C_{GD,i}$, $C_{GS,i}$, and $C_{DS,i}$, respectively. $L_{G,int,i}$, $L_{D,int,i}$, and $L_{S,int,i}$ represent the parasitic inductances of the pins of power devices mainly caused by the manufacturing technology and production process. $i_{D,i}$ is the drain current conducting the drain and common source parasitic inductances ($L_{D,i}$ and $L_{S,i}$, respectively) which are attributed to the PCB power circuit. $V_{dr,i}$ is the output driving voltage of the gate driver and $u_{GS,i}(t)$ is the gate-source voltage which is applied across $C_{GS,i}$. Finally, $di_{D,i}(t)/dt$ is the slew rate of the drain current.

$$i_{G,i} = i_{GD,i} + i_{GS,i} \tag{3}$$

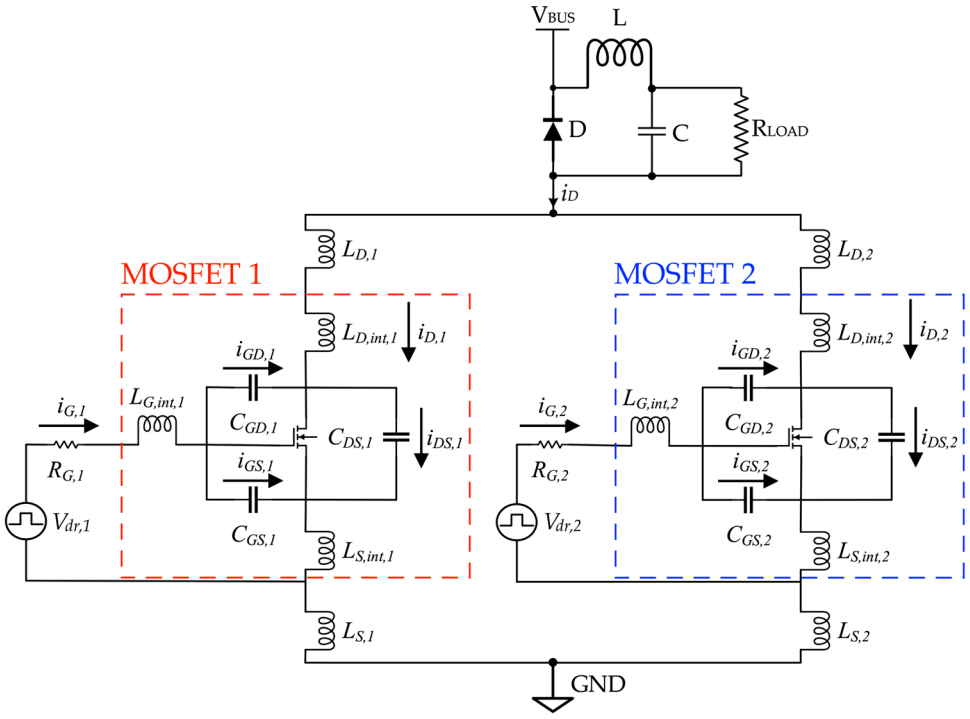


Figure 1. Equivalent circuit of two SiC MOSFETs connected in parallel, during transient stages, incorporated with a DC–DC buck converter.

As for the gate loop parasitic inductance ($L_{G,int,i}$), its effect on $V_{dr,i}$ can be neglected when the gate resistor $R_{G,i}$ is large enough. The Kirchhoff voltage equation for the gate drive current loop $i_{G,i}$ can be written as

$$i_{G,i} = \frac{V_{dr,i} - u_{GS,i}(t) - L_{S,int,i} \frac{di_{D,i}(t)}{dt}}{R_{G,i}} \quad (4)$$

As Equation (4) indicates, $i_{G,i}$ that charges and discharges $C_{GS,i}$, is affected by the $R_{G,i}$ magnitude, influencing the device behavior during transient stages. As a result, modifying the gate current by adjusting $R_{G,i}$ can lead to dynamic current imbalance suppression since di_D/dt and t_d of power devices tend to be synchronized.

According to ref. [34], transient imbalance can be suppressed by adjusting the time delays between power switches. Turn-on and -off delays ($t_{d,on}$ and $t_{d,off}$, respectively) can be directly affected by varying the firing angle (turn-on delay) and duty cycle (turn-off delay) of the PWM signal. During the turn-on interval, the SiC MOSFET which turns on faster is carried by a larger current than the other one. As a result, turn-on imbalance can be minimized by increasing the turn-on delay of the PWM controlling the fastest SiC MOSFET, forcing it to turn on slower. Contrariwise, during the turn-off interval, the power switch that turns off faster is carried by the least current compared to the other switch. The turn-off current imbalance can be reduced by increasing the turn-off delay of the PWM which drives the fastest SiC MOSFET, forcing it to turn off slower. Therefore, transient current imbalance can be suppressed with the proper adjustments of the turn-on and -off delays of the driving signals. Equations (5) and (6) express the total turn-on and -off time delays ($t_{d,on,total}$ and $t_{d,off,total}$, respectively). $t_{d,angle}$ and $t_{d,DC}$ represent the modifications of the firing angle and duty cycle, respectively.

$$t_{d,on,total} = t_{d,on} + t_{d,angle} \quad (5)$$

$$t_{d,off,total} = t_{d,off} + t_{d,DC} \quad (6)$$

To suppress current imbalance during turn-on and -off intervals, each dynamic imbalance requires different modifications and separate control for turn-on and -off intervals. This is attributed to different gate drive strengths and current/voltage waveforms at the drain [16].

2.2. Strategy of Static Current Imbalance Suppression

The equivalent circuit of two power devices during conduction stage, without the gate drivers, is shown in Figure 2. When V_{DS} across SiC MOSFET falls under the difference between the gate-source voltage and threshold voltage ($V_{GS} - V_{th}$), SiC MOSFET is treated as a resistance ($R_{DS\text{-}on,i}$, i = 1,2), as illustrated in Figure 2. $L_{D,i}$ represents the sum of the parasitic drain inductance and the one that is attributed to the PCB layout or the wiring. In addition, $L_{S,i}$ refers to the source terminal having the same meaning as $L_{D,i}$.

As pointed out earlier, steady-state imbalance is mainly caused by the $R_{DS\text{-}on}$ mismatch between power switches. On-resistance of SiC MOSFET shows a positive temperature coefficient (PTC), such as Si MOSFET. In this way, the junction temperature of the power switch carrying the largest current will increase, making its $R_{DS\text{-}on}$ greater. Therefore, static current imbalance could automatically be suppressed due to the thermal capability of Si MOSFET $R_{DS\text{-}on}$. However, SiC MOSFET $R_{DS\text{-}on}$ shows limited thermal sensitivity compared to Si ones [8]. As a result, the static current imbalance should be addressed in a different manner and without relying on the PTC characteristic of SiC MOSFET $R_{DS\text{-}on}$.

As mentioned above, during the steady-state, SiC MOSFET is equivalent to a resistance. For this reason, its drain current can be calculated by Equation (7) while static current

imbalance ($\Delta i_{D,static}$) for two SiC MOSFETs connected in parallel is expressed in Equation (8).

$$i_{DS} = \frac{V_{DS}}{R_{DS\text{-}on}} \tag{7}$$

$$\Delta i_{DS,static} = \frac{V_{DS}\Delta R_{DS\text{-}on}}{R_{DS\text{-}on,1}R_{DS\text{-}on,2}} \tag{8}$$

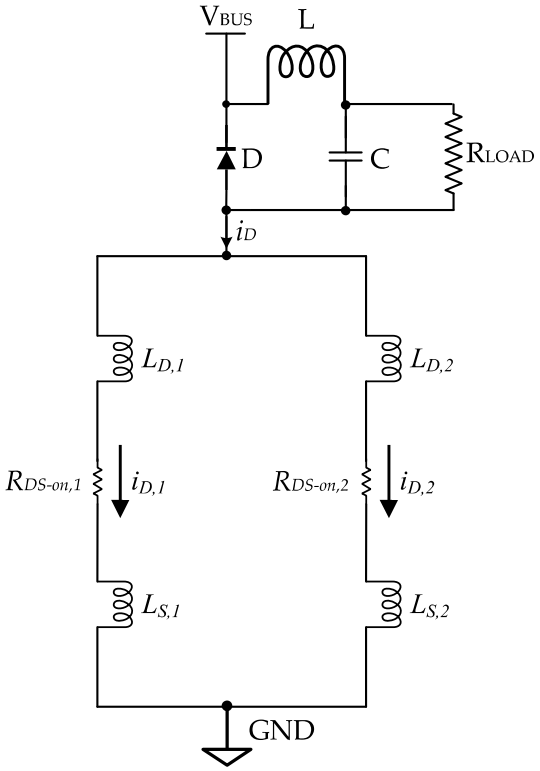


Figure 2. Equivalent circuit of two SiC MOSFETs connected in parallel, during conduction stage, incorporated with a DC–DC buck converter.

According to Equation (8), $\Delta i_{D,static}$ can be mitigated in case the $R_{DS\text{-}on}$ deviation ($\Delta R_{DS\text{-}on} = R_{DS\text{-}on,1} - R_{DS\text{-}on,2}$) between SiC MOSFETs becomes less. Based on [38], when an N-channel FET operates in the linear region, its drain current is expressed by Equation (9) where C_{ox} is the oxide capacitance, μ_n is the electron mobility, and L and W are the length and width of the gate.

$$i_D = \mu_n C_{OX}\frac{W}{L}[(V_{GS} - V_{th})V_{DS}] \quad when \quad V_{DS} \ll (V_{GS} - V_{th}) \tag{9}$$

By combining Equations (7) and (9), on-state resistance can be written as shown in Equation (10).

$$R_{DS\text{-}on} = \frac{1}{\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{th})} \tag{10}$$

Based on Equation (10), $R_{DS\text{-}on}$ magnitude can be controlled by V_{GS} while Equation (7) holds that the SiC MOSFET drain current depends on $R_{DS\text{-}on}$ during the steady-state. Therefore, $\Delta_{iD,static}$ can be minimized by properly varying the V_{GS} of the correct power device, leading to static current imbalance elimination.

However, modification of gate-source voltage V_{GS} affects not only static current imbalance but dynamic imbalance as well. According to [20], during the transient stage of the power switch, i_D satisfies the following relationship:

$$i_D = \begin{cases} 0 & V_{GS} < V_{th} \\ g_m(V_{GS} - V_{th}) & V_{th} < V_{GS} < V_{GP} \\ I_L & V_{GS} > V_{GP} \end{cases} \quad (11)$$

where I_L is the load current and V_{GP} is the plateau voltage caused by the Miller effect.

Based on Equation (11), dynamic current sharing is also influenced by V_{GS} difference (ΔV_{GS}) since the drain current is affected by V_{GS} during transient stages as well. However, it is not possible to eliminate the entire imbalance only by modifying V_{GS} because ΔV_{GS} has a different effect on each current imbalance.

For this reason, an efficient strategy is to eliminate static current imbalance by increasing ΔV_{GS} while transient imbalance should be mitigated by combining the two aforementioned transient imbalance suppression strategies.

3. Design of Active Current Balancing Technique

Since the current imbalance can be attributed to various factors, it is impossible to predict its type and magnitude. For this reason, static and dynamic current imbalances should be eliminated independently and regardless of the cause. In addition, the implementation of a current imbalance suppression technique should not require the knowledge of the technical parameters mismatch, current imbalance, and parasitic inductances between parallel SiC MOSFETs or the operating conditions. For this reason, the proposed technique is designed to address the current unbalance issue, fulfilling these requirements.

In this section, the operation principle and structure of the proposed technique are presented in detail. To address the current imbalance issue, the open-loop method is derived from two parts, as illustrated in Figure 3.

1. Gate driver: For every semiconductor device, an active gate driver (AGD) is utilized, capable of controlling power devices, and actively variate V_{GS} and R_G;
2. Digital controller: The PWM signals of the power devices are generated with the use of a digital controller. Additionally, the controller can control the parallel devices and eliminate the static and dynamic current imbalances by imposing the proper variations to several control parameters (V_{GS}, R_G, $t_{d,angle}$, and $t_{d,DC}$). Finally, the modification of the control parameters is realized manually through the digital controller.

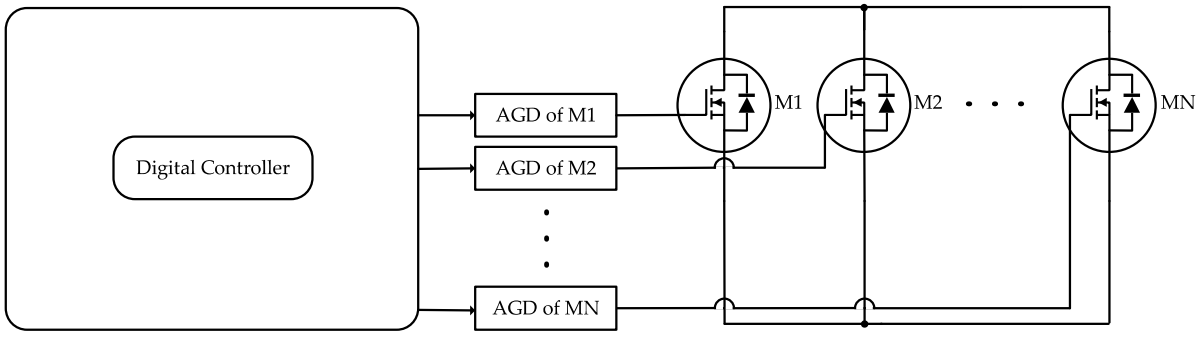


Figure 3. Application structure of the proposed active current balancing technique.

3.1. Capabilities and Structure of the Proposed Active Gate Driver

Based on the analysis of the previous section, all parameters affecting the current imbalance can be controlled by a gate driver and are related to the driving pulse generation source of the SiC MOSFETs. For this reason, an active gate driver is proposed capable of driving power devices and modifying these parameters to eliminate the current imbalance.

However, an active gate driver circuit is mandatory for every parallel-connected semiconductor device to apply different modifications to each SiC MOSFET control parameter.

3.1.1. Operation Principles of the Proposed Active Gate Driver

The proposed active gate driver includes a driving circuit to activate and deactivate the power device with the application of the V_{CC} and V_{EE} control voltages, respectively, as illustrated in Figure 4. Between the V_{CC} and the driving circuit, a forward converter is inserted to provide DC–DC isolation and actively modify the V_{CC} of SiC MOSFET by changing the PWM duty cycle (PWM_{VCC}) and controlling the forward converter switch. Duty cycle control is performed via the digital controller. As a result, the static current imbalance is eliminated by properly adjusting the correct V_{CC}.

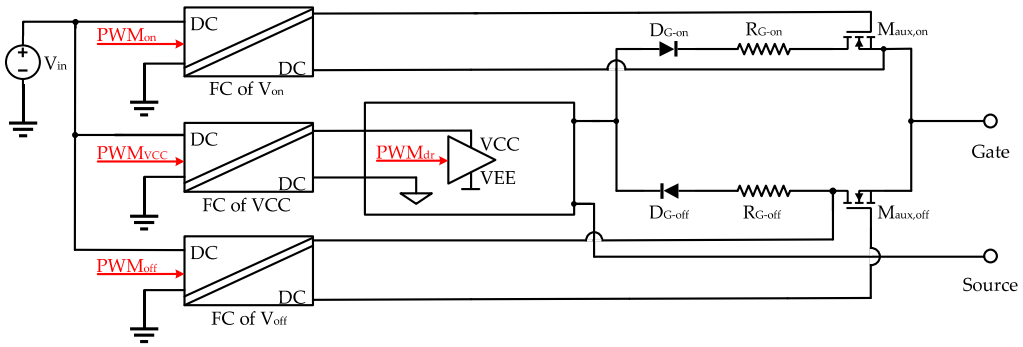


Figure 4. Proposed active gate driver circuit.

As pointed out in Section 2.1, dynamic current imbalance can be suppressed by properly varying the firing angle and duty cycle of the correct PWM_{dr} signal. However, it is not always possible to eliminate dynamic current imbalance by only changing these two control parameters. Varying the firing angle and duty cycle only affect the turn-on and -off processes of the power switch current, respectively, without influencing their current slopes. To sufficiently suppress dynamic current imbalance, turn-on and -off delays and current slopes should be properly adjusted. In conclusion, a great portion of the dynamic imbalance can be reduced through the variation in turn-on and -off delays. The remaining imbalance can be minimized with the proper adjustment of the gate current of the correct SiC MOSFET. As a result, this current balancing pattern offers the proposed technique the ability to mitigate any current imbalance independently and regardless of the cause.

3.1.2. Design of an Active Gate Driver

Variation in gate current can be achieved by changing the gate resistance size. As illustrated in Figure 4, the branch connected with the gate of SiC MOSFET is derived by two sub-branches which include a resistor ($R_{G\text{-}on}$ and $R_{G\text{-}off}$) connected in series with an auxiliary MOSFET ($M_{aux,on}$ and $M_{aux,off}$). Since the $R_{DS\text{-}on}$ of each MOSFET depends on its gate-source voltage, modifying the V_{GS} of each auxiliary MOSFET changes the entire resistance of each branch. In this way, the turn-on and -off delays and the current slope of the power device are affected. The upper and lower branch control the charging and discharging gate current, respectively. In each branch, a diode ($D_{G\text{-}on}$ and $D_{G\text{-}off}$) is series-connected with their elements to independently control the charging and discharging currents. The control voltages of $M_{aux,on}$ and $M_{aux,off}$ are modified with the aid of two other forward converters with the control of the duty cycles of the PWM_{on} and PWM_{off} signals, respectively. In conclusion, each subbranch is treated as a voltage-controlled gate current source.

Therefore, the gate-source voltage of each MOSFET can be modified through the duty cycle, controlling the switch of each forward converter. The duty cycle control of each PWM signal is performed through the digital controller. Finally, the control of the power

device along with the forward converter switches requires four different driving pulses for each parallel power device.

3.1.3. Forward Converter Design Guidelines

The elimination of every current imbalance type is influenced by the digital controller's maximum clock frequency. Each PWM signal is generated with the aid of a step-up counter which includes a reset capability. As illustrated in Figure 5, the counter increases by one step for every positive edge of the clock and resets when it reaches a certain value.

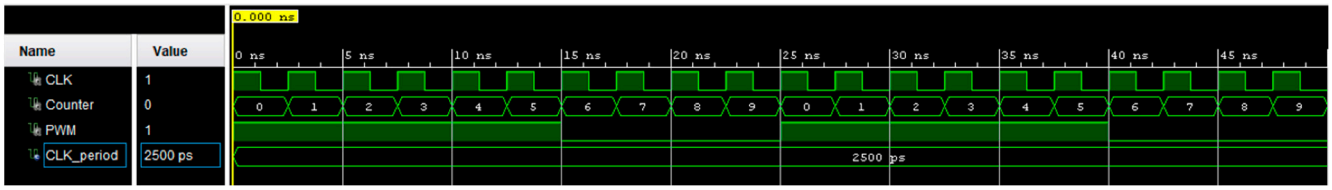


Figure 5. PWM generation strategy.

Therefore, PWM frequency and duty cycle are set based on this function. As depicted in Figure 5, when the counter does not reach a specific value (e.g., lower than 6), PWM turns "high", but when it reaches and exceeds a limit (e.g., 6 or higher), it turns "low". For a specific time period, the count times of the counter increase as the clock frequency becomes higher. In this way, the minimum variations of the turn-on and -off delays are decreased. As a result, the minimization of dynamic current imbalance by adjusting the turn-on and -off delays can become even more efficient. Additionally, the minimum variation step of each gate-source voltage decreases, making the current balancing process even more reliable. The minimum modification step on the control voltage ($V_{var,step}$) can be expressed by Equation (12) where f_{clk}, V_{out}, and f_{sw} are the clock frequency of each counter, the output voltage, and the forward converter switching frequency, respectively. As a result, the minimum variation on the output voltage can be reduced with the usage of a digital controller with a high clock frequency capability while the forward converter frequency (f_{sw}) should be kept low. On the other hand, digital controllers with ultra-high fundamental frequency (f_{clk}) are expensive. In conclusion, the selection of f_{sw} is a trade-off between the current balancing process reliability and the implementation cost of the proposed technique.

$$V_{var,step} = \frac{V_{out} f_{sw}}{f_{clk}} \tag{12}$$

In practice, one crucial matter is the design of the forward converter regarding the reset method of the transformer core. For this reason, a two-switch forward converter topology with two MOSFET switches Q_1 and Q_2 is used, as shown in Figure 6. Both switches are controlled by one gate driver circuit which is derived from the R_{HI}, R_{LI}, D_{BOOT}, C_{BOOT}, and Gate Driver IC elements and simultaneously turns both switches on and off. This method manages to reset the transformer core by using two demagnetization diodes D_1 and D_2. When the switches are turned off, the demagnetization diodes become forward biased and the magnetizing energy in the transformer is returned to the input voltage source (V_{in}) [39].

In addition, R_1 and C_1 and R_2 and C_2 are the snubbing elements connected in parallel with the secondary diodes (D_3 and D_4) to dampen the oscillations that appear across them. These oscillations are attributed to the leakage inductance of the secondary side of the transformer with the capacitor behavior of the diodes when they are blocked. The oscillations take place at the end of the diode conduction.

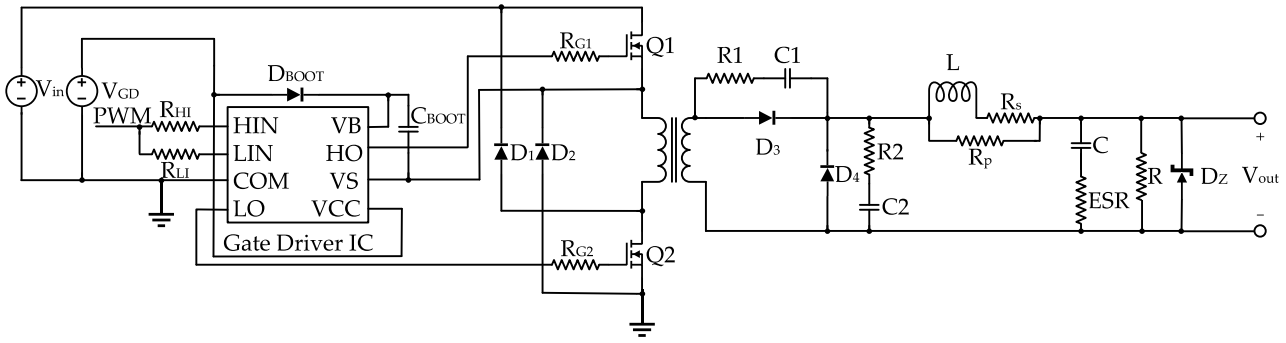


Figure 6. Two-switch forward converter topology.

Another essential matter is the output voltage ripple which is strongly dependent on the inductor (L) and capacitor (C) magnitudes. R_S is the inductor equivalent series resistance and R_p is the parallel resistance correlated with the parallel leakage path across the inductor. Also, *ESR* is the capacitor series resistance. Each forward converter has a Zener diode (D_Z) connected in parallel with the load resistance (R). According to Equation (13), the reduction in output inductor current ripple (ΔI_{LX}) can be achieved by increasing the switching frequency. However, Equation (12) states that $V_{var,step}$ increases when f_{sw} becomes larger. Additionally, ΔI_{LX} is affected by the inductor size while Equation (14) states that the output voltage ripple (ΔV_{out}) is affected by the capacitor value. Therefore, *LC* filter values should be properly chosen to reduce ΔV_{out} since ΔI_{LX} and ΔV_{out} can be decreased as the inductor and capacitor increase. However, the inductor affects the converter output voltage because of the voltage drop caused by its parasitic resistance which becomes larger as the inductor size increases. In addition, the output voltage depends on the load current which lowers as the inductor becomes larger. As for the capacitor, its value should be selected concerning the response time of the converter to the duty cycle (D) variations which increase as the capacitor becomes larger. Finally, R should be as large as possible for lowering converter power consumption, taking into account the fact that the R value affects the converter response time.

In conclusion, the forward converter should offer an output voltage with a low ripple. Also, the output voltage should be able to vary in a quite short period of time (mseconds) which is a trade-off between the *LC* filter and switching frequency.

$$\Delta I_{LX} = \frac{V_{out}\,(1-D)}{L f_{sw}} \tag{13}$$

$$\Delta V_{out} = \Delta I_{LX}\left(\frac{1}{8\,C\,f_{sw}} + ESR\right) \tag{14}$$

3.2. Functions of the Digital Controller

To address the current imbalance issue, the digital controller includes a number of functions. Initially, the digital controller generates the driving pulses for the control of the SiC MOSFETs with a controllable switching frequency and duty cycle. In addition, the digital controller generates three PWM signals with a fixed frequency and an initial duty cycle which can be modified with the purpose of varying the V_{CC} of power devices and the control voltages of the auxiliary MOSFETs to affect the gate currents. Finally, the duty cycle and turn-on delay of each power switch PWM signal can also be modified.

Current Imbalance Suppression Methodology

To eliminate the entire imbalance, a current balancing methodology should be followed. Before applying any necessary correction to the control parameters of the appropriate power device(s), it is necessary to identify the polarities of the three imbalances.

In the process, all three imbalances should not be suppressed simultaneously but in a specified order, as depicted in Figure 7. If the static current imbalance is larger than a certain value (e.g., 0.1A), the V_{CC} of the SiC MOSFET with the lowest current should start to increase with the purpose of lowering its on-resistance. In case V_{CC} reaches a specific limit and static imbalance remains, the V_{CC} of the SiC MOSFET with the highest current should start to decrease until on-resistances become equal. Otherwise, static current imbalance can also be eliminated by decreasing only the V_{CC} of the SiC MOSFET with the highest current.

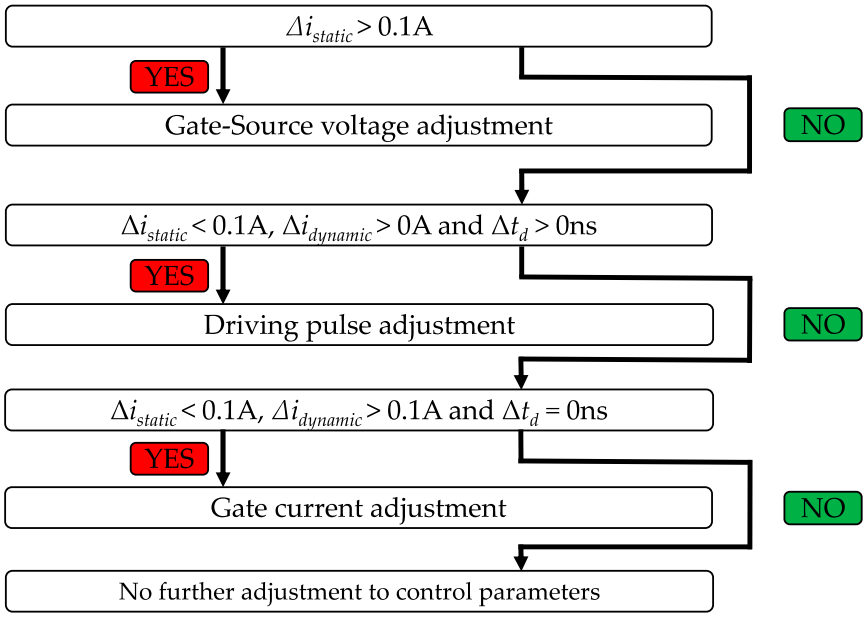


Figure 7. Current balancing strategy flow.

Once static current imbalance becomes less than a certain threshold, if there is dynamic imbalance ($\Delta i_{dynamic}$) a certain balancing order should be executed. Dynamic current balancing can be achieved by forcing the peak currents during turn-on and -off intervals ($\Delta i_{D,on}$ and $\Delta i_{D,off}$) to match. If $\Delta i_{D,on}$ and turn-on delay difference ($\Delta t_{d,on}$) between parallel currents are greater than zero, the turn-on delay ($t_{dl,on}$) of the PWM signal driving the power switch with the largest current during the turn-on transience should begin to increase. Whether $\Delta i_{D,on}$ is eliminated or $\Delta t_{d,on}$ becomes zero, modification of turn-on delay should cease to increase. In case the turn-on imbalance still exists, the charging gate current of the SiC MOSFET, carrying the highest current, should start to become less by decreasing the V_{GS} of the appropriate auxiliary MOSFET until the turn-on peak current difference is minimized.

As for the elimination of the turn-off dynamic imbalance, if $\Delta i_{D,off}$ and turn-off delay difference ($\Delta t_{d,off}$) between parallel currents are greater than zero, the duty cycle of the PWM controlling the power switch with the lowest current during turn-off should start to increase by $t_{dl,off}$. Either $\Delta i_{D,off}$ is minimized or $\Delta t_{d,off}$ becomes zero; the variation in the duty cycle should be ceased. If the turn-off dynamic imbalance remains, the charging gate current of the power device with the least current during the turn-off interval should become less by lowering the V_{GS} of the correct auxiliary MOSFET until the difference between peak currents is minimized.

In any case, the balancing process should always be executed following this pattern. When there is a static current imbalance, the two transient imbalances include both static and dynamic imbalances. Also, the modification of V_{CC} affects not only static imbalance but also dynamic imbalance as well. This may force the dynamic current imbalances to change polarity, especially when the modification of V_{CC} is too large. If this precaution is not taken, it is difficult or even impossible to discover and impose the proper modifications to the control parameters of the correct power device to suppress dynamic imbalances.

4. Test Platform and Experimental Results

4.1. Test Platform

In previous work, the effectiveness and durability of the proposed technique against current imbalance were tested through simulation tests eliminating current imbalance automatically [40,41]. To experimentally verify the effectiveness of the proposed current balancing technique, an experimental test platform is constructed. The structure of the test platform and the proposed current balancing system are depicted in Figure 8. Table 1 lists all the equipment used. The test platform is derived by a DC–DC buck converter with two SiC MOSFETs C2M0080120D (M1 and M2) connected in parallel. As a free-wheeling diode, SiC Schottky E4D20120D is used. The power converter supplies a resistive load while an *LC* filter is used for smoothing the output voltage. The realization of the proposed method includes the digital controller, two current sensors, and two active gate driver circuits which are powered by a separate DC power supply. All the capabilities of the digital controller can be realized with an algorithm and executed with an FPGA (field programmable gate array). For this reason, the Nexys A7-100T FPGA trainer board is used which includes the FPGA Artix-7 offering a clock speed of 500 MHz. Also, an algorithm is written in the VHDL programming language to execute all the digital controller functions. Since two gate drivers are utilized, the FPGA generates eight PWMs for the control of the power devices and the forward converters. The FPGA algorithm utilizes 14 switches (SW), the 7-segment displays, and the pushbuttons of the FPGA board. Table 2 mentions in detail the function of each FPGA switch. The control results of the switching frequency and duty cycle of the SiC MOSFETs as well as the control parameters are displayed in the FPGA 7-segment displays and controlled with the help of the pushbuttons. Finally, the measurement of each drain current is achieved with a surface mount resistor R_{sense} of 100 mΩ and 1 W, connected in series with the source pin of each parallel power device.

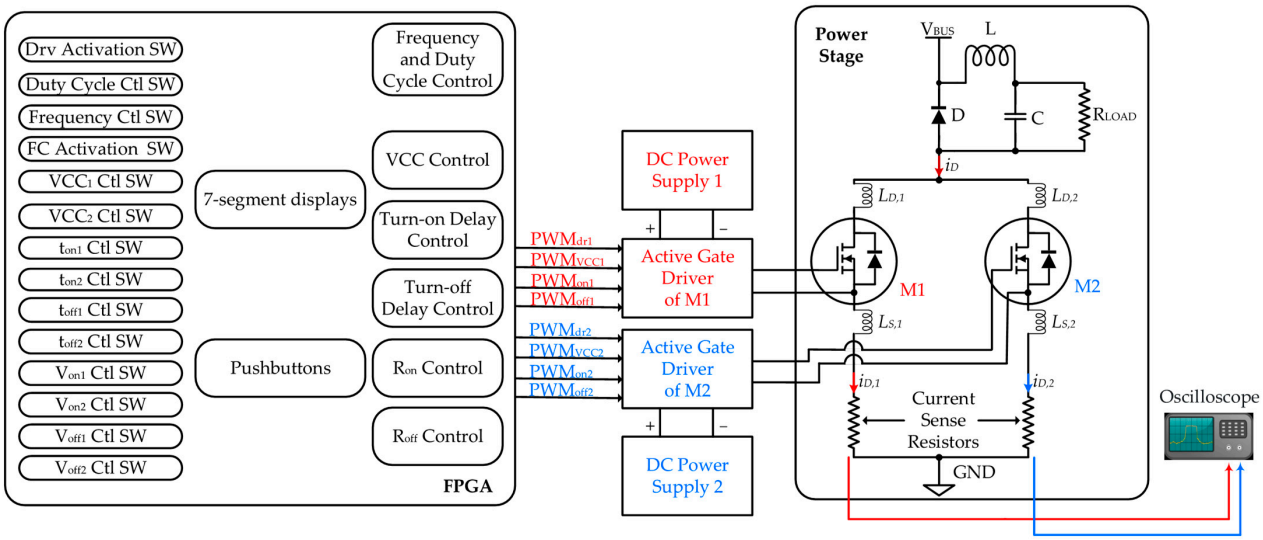


Figure 8. Application of the proposed method for two parallel-connected SiC MOSFET.

Table 1. Equipment used in the experimental tests.

Equipment	Model	Bandwidth	Function
Digital oscilloscope	Keysight MSOX3014A	100 MHz	Capture curves
Current Sense Resistor	LTR10LEZPFLR100	-	Measure I_D
BNC Coaxial cable	141-12BM+	3 GHz	Measure I_D and I_G
BNC Coaxial connector	CONBNC002	1 GHz	Measure I_D and I_G
Voltage probe	Agilent N2862A	150 MHz	Measure V_{GS} and V_{DS}

Table 2. Functions of FPGA Switches.

Switch	Function
Drv Activation SW	Activation driving of SiC MOSFETs
Duty Cycle Ctl SW	Duty cycle control of SiC MOSFETs
Frequency Ctl SW	Switching frequency control of SiC MOSFETs
FC Activation SW	Activation driving of forward converters
VCC_1 Ctl SW	V_{CC} control of M1
VCC_2 Ctl SW	V_{CC} control of M2
t_{on1} Ctl SW	Turn-on delay control of M1
t_{on2} Ctl SW	Turn-on delay control of M2
t_{off1} Ctl SW	Turn-off delay control of M1
t_{off2} Ctl SW	Turn-off delay control of M2
V_{on1} Ctl SW	Control of Gate-Source voltage of $M_{aux,on,1}$
V_{on2} Ctl SW	Control of Gate-Source voltage of $M_{aux,on,2}$
V_{off1} Ctl SW	Control of Gate-Source voltage of $M_{aux,off,1}$
V_{off2} Ctl SW	Control of Gate-Source voltage of $M_{aux,off,2}$

The DC bus power supply (V_{BUS}) of the DC–DC buck converter is implemented using a three-phase full-bridge diode rectifier which is connected in parallel with two capacitors (1500 µF/550 V) to smooth the output voltage of the bridge. The DC bus power supply also consists of a protection system that includes a resistor of 3.3 kΩ/10 W. When the resistor is connected in parallel with the capacitors, it discharges them for safety purposes. As shown in Figure 9, the operation of the entire platform is controlled by a relay (Rel) which is powered by a single-phase AC power supply of 230 V. Once the switch (SW) is closed and the AC supply is ON, the relay connects the three-phase power supply with the rectifier bridge through a normally open (NO) three-phase switch, and at the same time disconnects the discharging resistor from the capacitors through a normally closed (NC) single-phase switch. Otherwise, the relay disconnects the bridge with the three-phase AC supply and connects the discharging resistor with the capacitors. In addition, four electric fuses are used, three in the three-phase AC supply (F1, F2, and F3) and one in the single-phase AC supply (F4), offering overcurrent protection to the experimental platform. The constructed experimental test platform is shown in Figure 10.

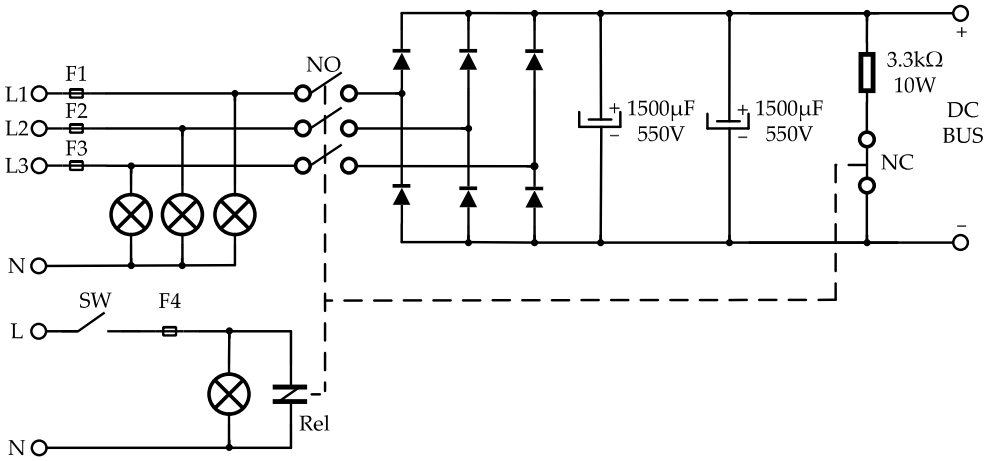


Figure 9. Power supply circuit consists of a three-phase rectifier, a smoothing filter, and a protection circuit.

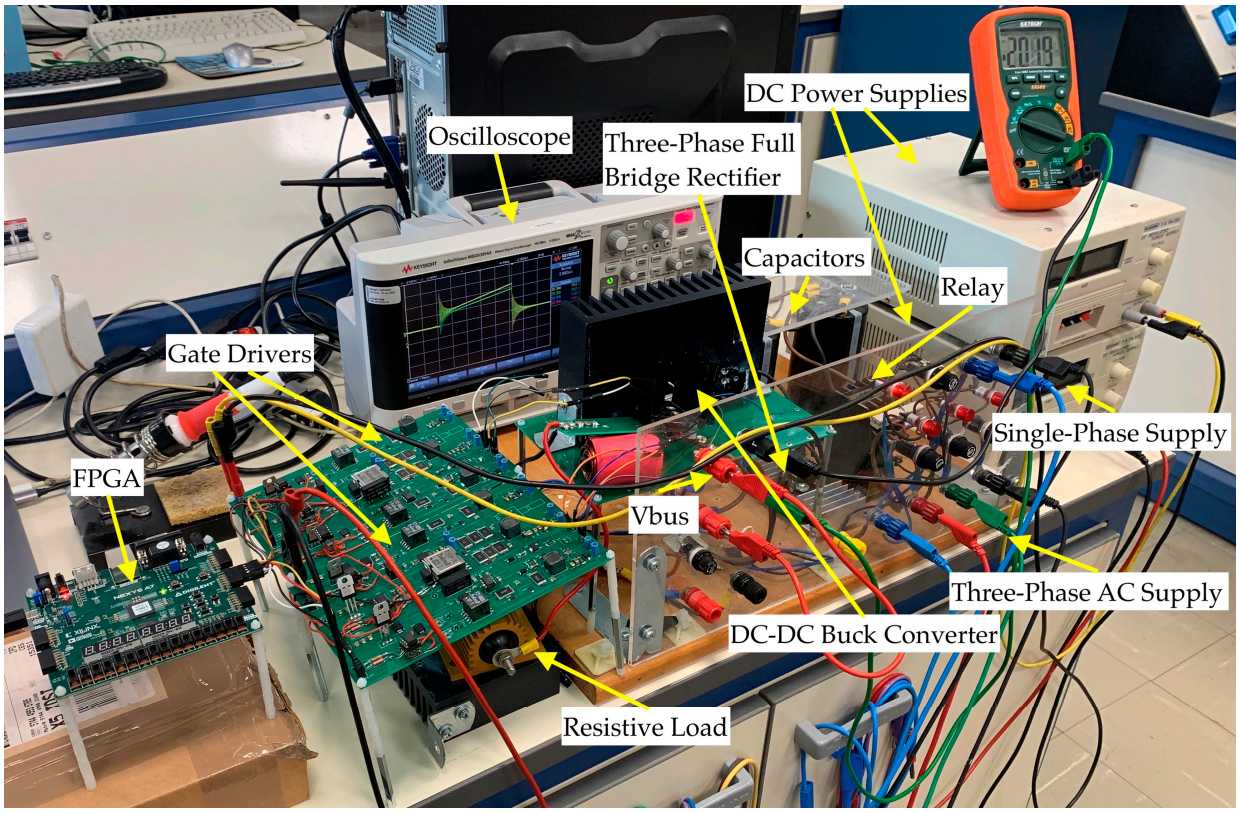


Figure 10. Test platform for the proposed current balancing method.

As for the test conditions, the buck converter operates under a DC bus voltage of 200 V with a frequency and duty cycle of 25 kHz and 25%, respectively, supplying a load of 10 Ω. The initial V_{dr} values for activating and deactivating each parallel SiC MOSFET are 20 V and −5 V, respectively. Finally, $R_{G\text{-}on}$ and $R_{G\text{-}off}$ are equal to 10 Ω while the gate-source voltages of $M_{aux,on}$ and $M_{aux,off}$ are set to 9 V. $V_{ctl\text{-}M,on,i}$ and $V_{ctl\text{-}M,off,i}$ are the output voltages of the forward converter of $M_{aux,on}$ and $M_{aux,off}$, respectively.

The initial values of the activation and deactivation voltages were selected as 20 V and −5 V, respectively, recommended by the datasheet of the utilized SiC MOSFETs C2M0080120D. The manufacturing company (Wolfspeed) has constructed a gate driver (CGD15SG00D2) designated for the driving of that particular SiC MOSFET model. CGD 15SG00D2 uses an isolated DC/DC converter to generate two output voltages of 20 V and −5 V while its output power is 2 W with an efficiency of 86%, meaning that the input power of the driver is 2.3 W. On the other hand, the input voltage (V_{in}) of our proposed gate driver is 17 V to supply all three forward converters and an isolated DC/DC converter that generates the deactivation voltage of 5 V which is always constant. In case the FPGA controls only the forward converter which generates the activation voltage at 20 V, the input current is measured to be 0.15 A. Therefore, the input power of the proposed active gate driver when it supplies constant activation and deactivation voltages is almost 2.5 W, which is very close to the input power of the commercial gate driver (CGD15SG00D2). In case the FPGA controls all forward converters and the output voltages that control auxiliary MOSFETs are 9 V, the overall input current and power of the active gate driver are 0.21 A and 3.6 W, respectively. Therefore, both forward converters and the auxiliary MOSFETs add only 1.1 W of power consumption compared to the previous case in which the proposed active gate driver works in a similar way to the commercial driver. In the worst-case scenario, when the activation voltage reaches 23 V for the suppression of static imbalance, the input current and power are 0.29 A and 4.9 W, respectively.

4.2. Current Sensing System Accuracy

The current measurement of SiC MOSFETs requires sensors of high bandwidth because of their fast-switching speed. Based on [42], surface mount resistors can offer exceptional measurement accuracy since their bandwidth can be on the order of hundreds of megahertz. One of the most important factors affecting their bandwidth is parasitic inductance which is inevitable because of the magnetic field induced by the current conducting the sensor [43]. For this reason, surface mount resistor size should be as low as possible to provide low parasitic inductance in the order of nano or even picohenry. Also, R_{sense} should have low resistance without significantly affecting the current level and offering quite low power losses. On the other hand, one of the pulse current measurement methods that are strongly recommended for the current measurement of WBG devices is the coaxial shunt resistors which can offer MHz or even GHz measurement bandwidth.

To examine the measurement accuracy of the utilized current sensor, two experimental tests are performed, measuring the current of one SiC MOSFET. In the first test, the power switch current is measured with the surface mount resistor of 100 mΩ. In the process, the SiC MOSFET current is measured with the coaxial shunt resistor SDN-414-01 which offers a measurement bandwidth of 400 MHz. The voltage developed across the current sense resistor is illustrated to the oscilloscope with the aid of a BNC coaxial connector and a BNC coaxial cable of quite high bandwidth, as shown in Table 1. Figure 11 depicts and compares the current waveforms of both tests during the conduction stage as well as the turn-on and -off intervals, demonstrating the surface mount resistor measurement accuracy. Compared to the coaxial shunt resistor, the surface mount resistor only shows a measurement delay of around 5 ns during the current ringing stages. However, this time delay difference can be ignored because both waveforms are identical during the rising, conduction, and falling stages of the drain current. In conclusion, for the purposes of this research, the current sense resistor offers high enough measurement accuracy of the drain current of SiC MOSFET.

4.3. Experimental Test Results

In this subsection, the effectiveness of the proposed method is tested by performing two experimental tests. In the first test, a pair of devices is connected in parallel causing current imbalance during steady and dynamic stages which may be attributed to the variation in the technical parameters between SiC MOSFETs. PCB layout of the power circuit is designed to be symmetrical to minimize the length differences between PCB traces to exclude any current imbalance attributed to mismatched parasitic inductances. In the second test, another pair of devices is connected in parallel which originally shows an equal current sharing between power devices. However, the layout was designed to be asymmetrical by connecting the power devices with different gate, drain, and source pin lengths. This leads to static and dynamic current imbalance caused mainly by the mismatch of the drain and common source parasitic inductances. Ref. [31] argues that the mismatch of gate parasitic inductances has an almost negligible effect on dynamic current sharing. The experimental results are further compared under different test conditions (a) without and (b) with the proposed current balancing technique. Figure 12 depicts the drain-source voltage (V_{DS}), developed across power devices, during the conduction stage and the turn-on and -off transitions. The experimental results of the two tests are illustrated in Figures 13–18, depicting the drain currents of the parallel-connected SiC MOSFETs as well as their turn-on and -off gate currents and driving signals. Tables 3 and 4 report the imposed modifications to the control parameters to balance the parallel currents.

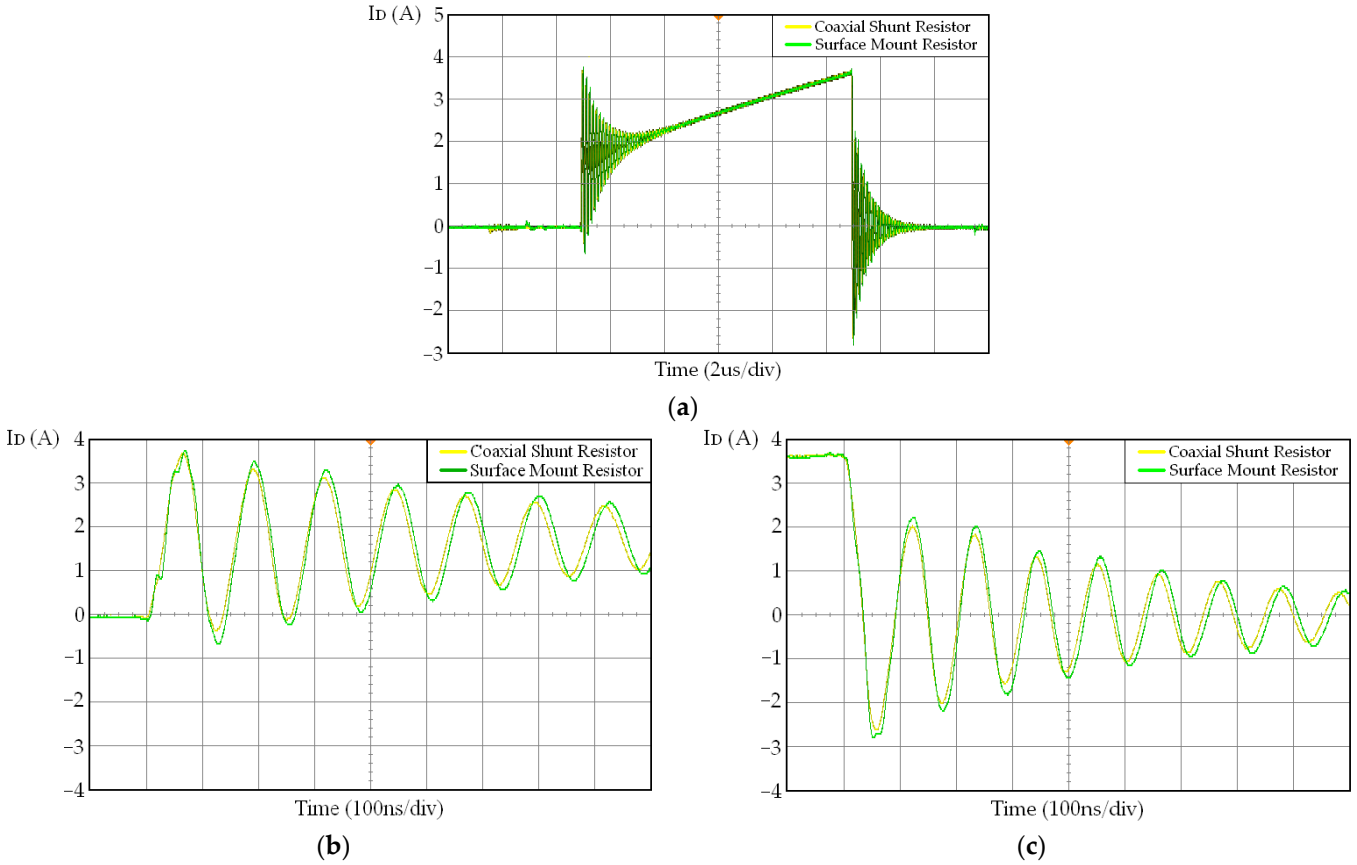


Figure 11. Experimental comparison of current measurement accuracy between the coaxial shunt resistor SDN-414-01 and the surface mount resistor of 100 mΩ during the: (**a**) conduction stage; (**b**) turn-on transition; and (**c**) turn-off transition.

Table 3. Modifications upon control parameters (a) without and (b) with the proposed method of the first experimental test.

a/a	$V_{CC,1}$ (V)	$V_{CC,2}$ (V)	$t_{dl,on,1}$ (ns)	$t_{dl,on,2}$ (ns)	$t_{dl,off,1}$ (ns)	$t_{dl,off,2}$ (ns)	$V_{ctl\text{-}M,on,1}$ (V)	$V_{ctl\text{-}M,on,2}$ (V)	$V_{ctl\text{-}M,off,1}$ (V)	$V_{ctl\text{-}M,off,2}$ (V)
(a)	20	20	0	0	0	0	9	9	9	9
(b)	12.5	23	0	22	0	6	9	9	9	9

Table 4. Modifications upon control parameters (a) without and (b) with the proposed method of the second experimental test.

a/a	$V_{CC,1}$ (V)	$V_{CC,2}$ (V)	$t_{dl,on,1}$ (ns)	$t_{dl,on,2}$ (ns)	$t_{dl,off,1}$ (ns)	$t_{dl,off,2}$ (ns)	$V_{ctl\text{-}M,on,1}$ (V)	$V_{ctl\text{-}M,on,2}$ (V)	$V_{ctl\text{-}M,off,1}$ (V)	$V_{ctl\text{-}M,off,2}$ (V)
(a)	20	20	0	0	0	0	9	9	9	9
(b)	20	17	11	0	4	0	6.5	9	4.8	9

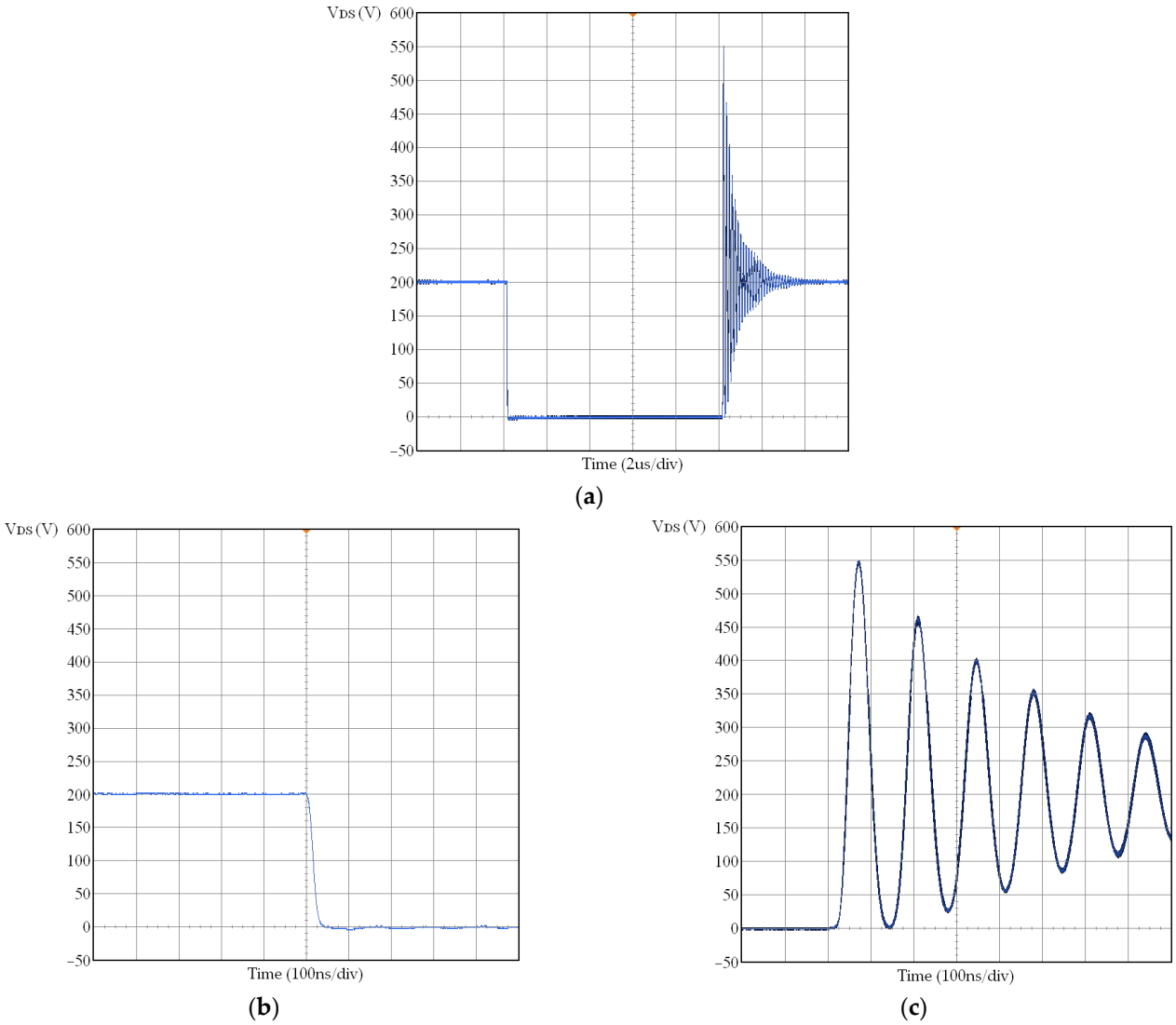
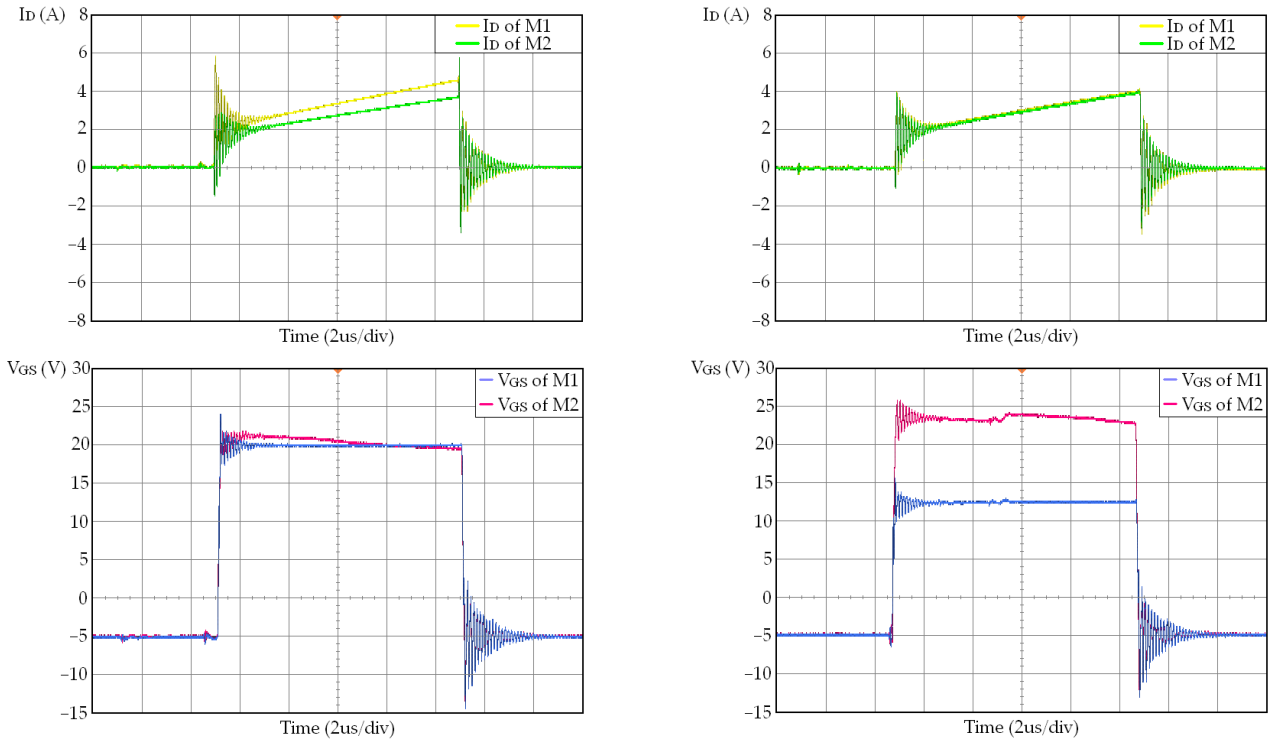


Figure 12. Drain–source voltage during the: (**a**) conduction stage; (**b**) turn-on transition; and (**c**) turn-off transition.

Current imbalance levels (ΔI_D) are mentioned in Tables 5 and 6 for both tests without and with the proposed solution. Based on the experimental results, the current curves and peak currents (I_{Dmax}) between the parallel power devices are almost the same.

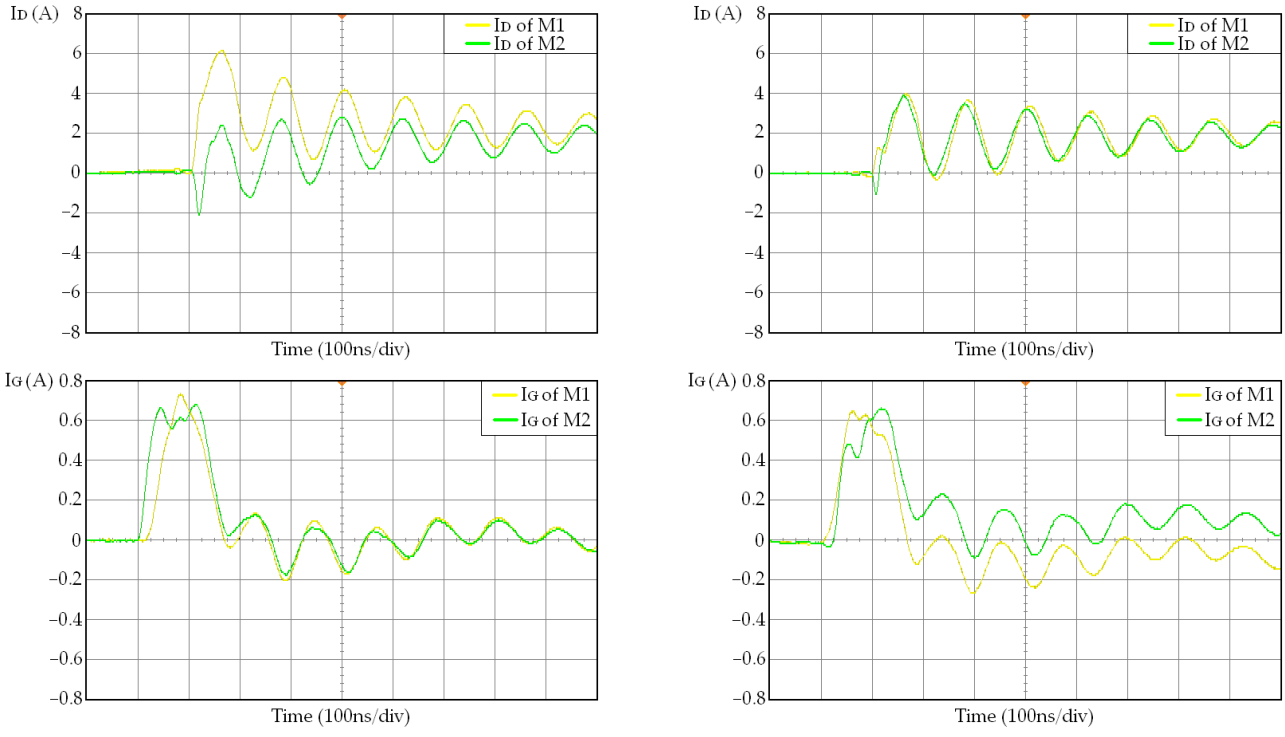
Table 5. Comparison of experimental results for the first test.

Condition	Device	Turn-on		Steady-State		Turn-off	
		I_{Dmax} (A)	ΔI_D (A)	I_{Dmax} (A)	ΔI_D (A)	I_{Dmax} (A)	ΔI_D (A)
Without solution	M1	6.2	3.8	4.55	0.9	4.7	1.1
	M2	2.4		3.65		5.8	
With the proposed method	M1	4	0.1	4	0.1	4.2	0.1
	M2	3.9		3.9		4.1	



(**a**) (**b**)

Figure 13. Drain to source currents and driving signals of the first experimental test: (**a**) without; and (**b**) with the proposed current balancing technique.



(**a**) (**b**)

Figure 14. Drain and gate currents of the first experimental test during turn-on transition: (**a**) without; and (**b**) with the proposed current balancing technique.

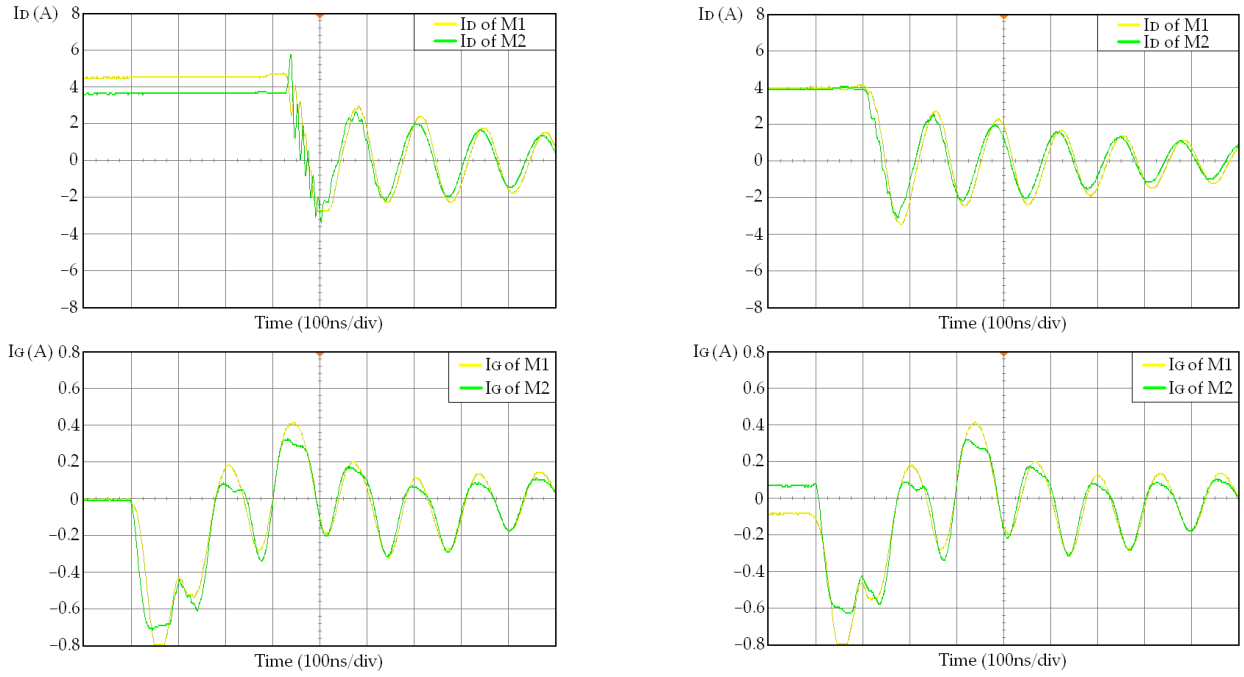


Figure 15. Drain and gate currents of the first experimental test during turn-off transition: (**a**) without; and (**b**) with the proposed current balancing technique.

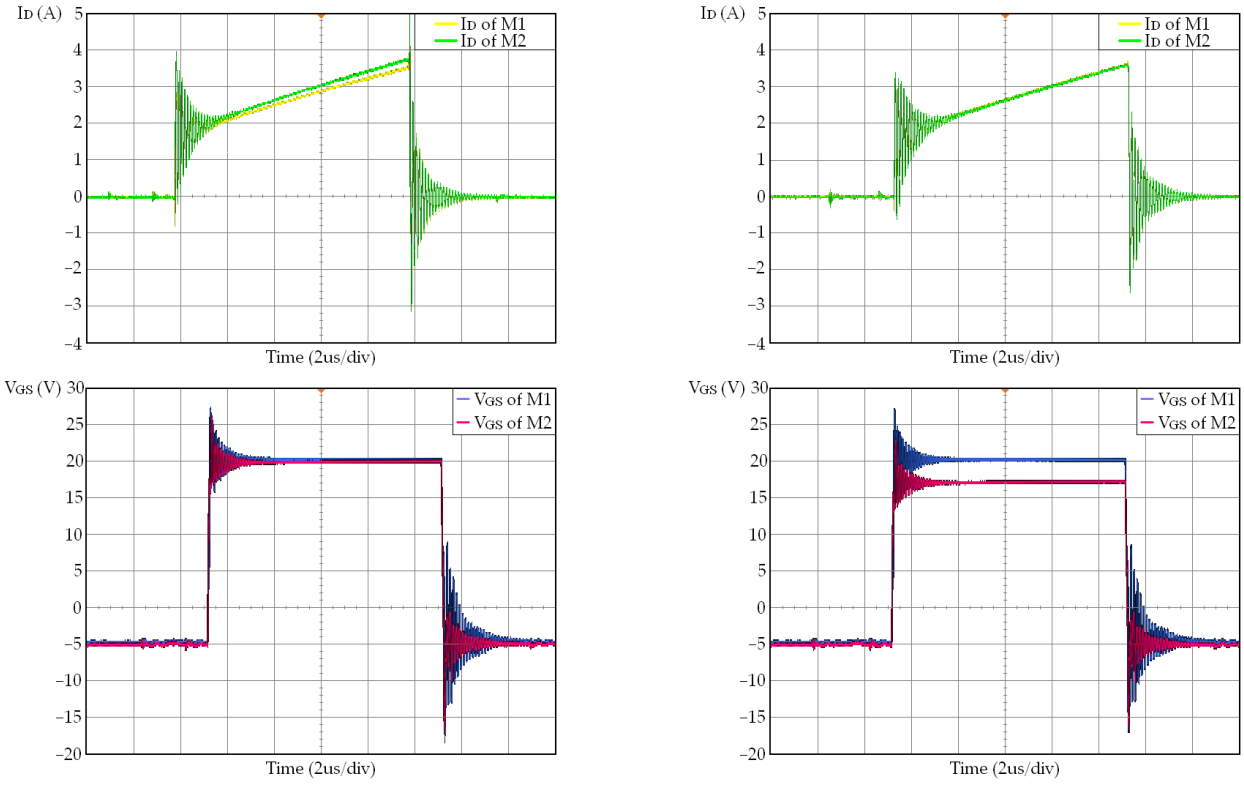
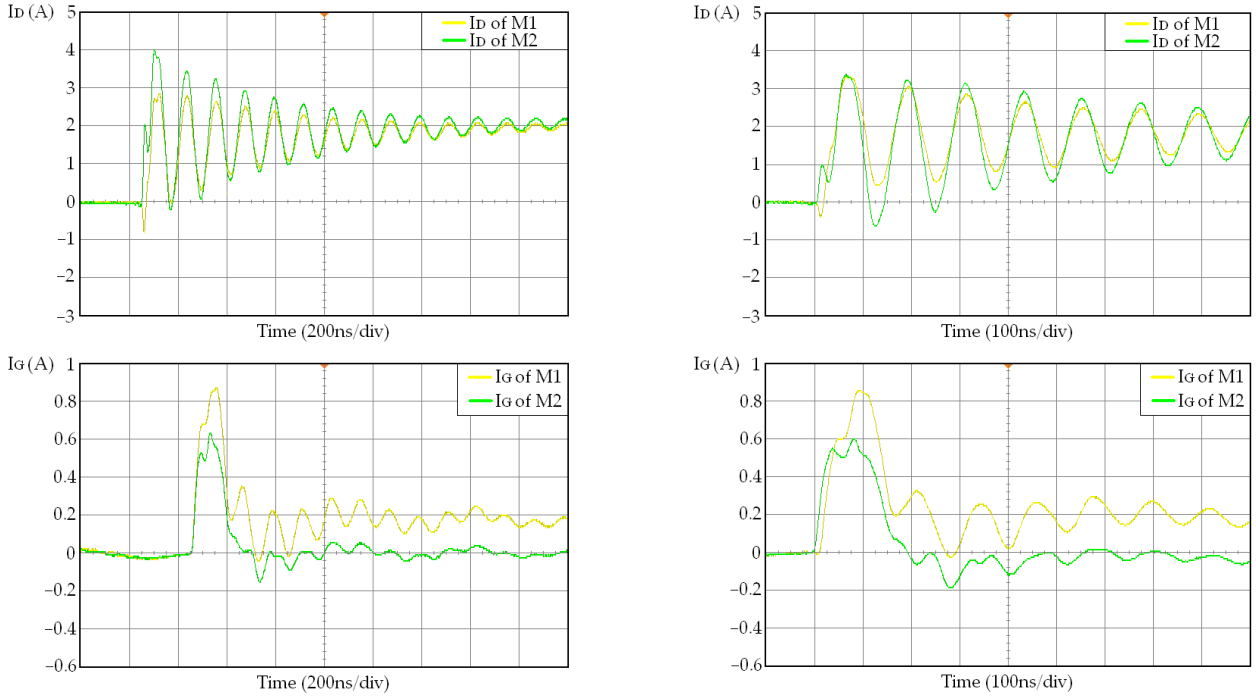
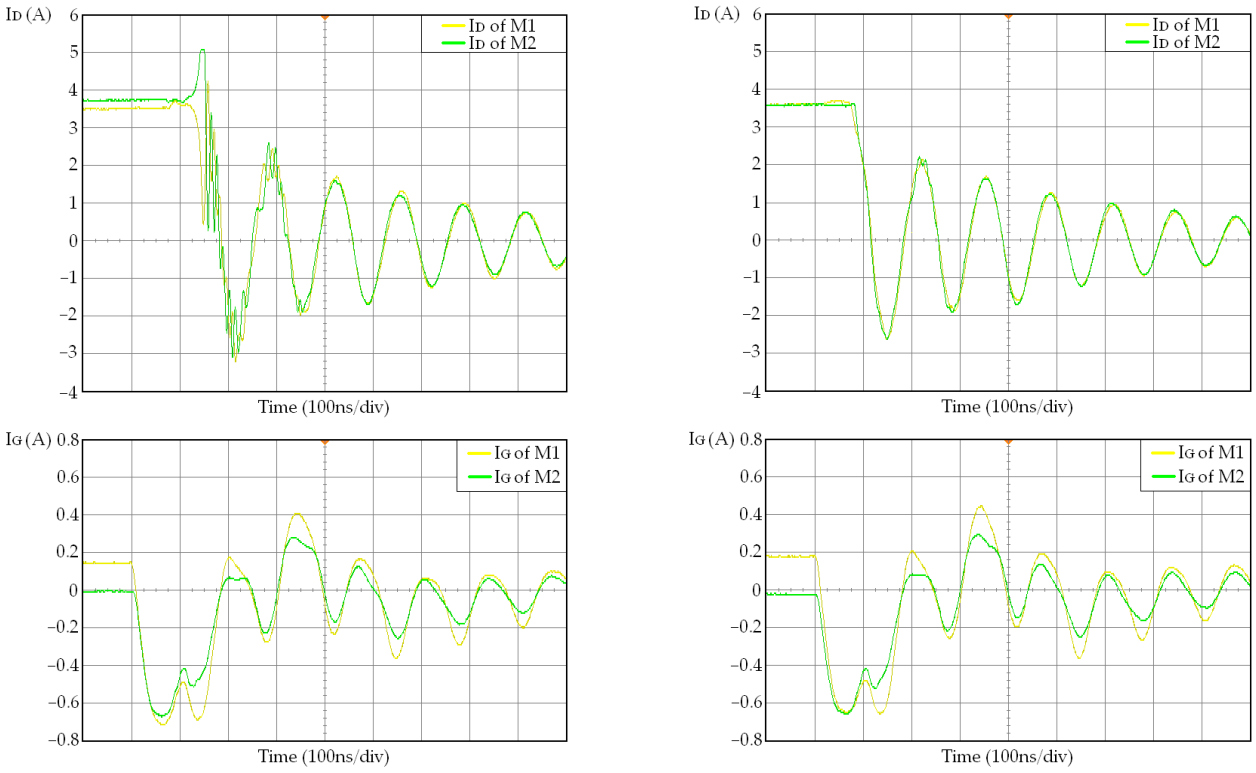


Figure 16. Drain to source currents and driving signals of the second experimental test: (**a**) without; and (**b**) with the proposed current balancing technique.



(**a**) (**b**)

Figure 17. Drain and gate currents of the second experimental test during turn-on transition: (**a**) without; and (**b**) with the proposed current balancing technique.



(**a**) (**b**)

Figure 18. Drain and gate currents of the second experimental test during turn-off transition: (**a**) without; and (**b**) with the proposed current balancing technique.

Table 6. Comparison of experimental results for the second test.

Condition	Device	Turn-on		Steady-State		Turn-off	
		I_{Dmax} (A)	ΔI_D (A)	I_{Dmax} (A)	ΔI_D (A)	I_{Dmax} (A)	ΔI_D (A)
Without solution	M1	2.85	1.15	3.45	0.3	3.7	1.4
	M2	4		3.75		5.1	
With the proposed method	M1	3.3	0.1	3.6	0.05	3.7	0.1
	M2	3.4		3.65		3.6	

In the first test, by implementing the proposed method, turn-on and -off imbalances are reduced from 44% to 1.3% and 10.5% to 1.2%, respectively, while the static imbalance is decreased from 11% to 1.3%. In the second test, turn-on and -off imbalances are reduced from 16.8% to 1.5% and 15.9% to 1.4%, respectively, while the static imbalance is decreased from 4.2% to 0.7% (((0.05 × 100)/(3.65 + 3.6)) × 100% = 0.7%).

According to the experimental results, before applying the proposed innovative technique, a significant amount of current imbalance is shown between the drain currents during all device stages. However, the proposed method can offer a well-balanced current sharing between SiC MOSFETs by properly adjusting the correct control parameters, proving its current balancing performance against multiple impact factors and promoting the safety of the parallel SiC MOSFETs.

The pair of SiC MOSFETs that were used for the first experimental test was determined through a number of tests, connecting several pairs of SiC MOSFETs in parallel. We have reached the decision to use this particular pair of SiC MOSFETs due to the large static and dynamic current imbalances that occur. Both imbalances may be attributed to the deviation of the technical parameters between parallel devices. Such static current imbalance can only be caused due to the on-resistance difference of the SiC MOSFETs. For this reason, the elimination of the static current imbalance was only possible by driving the parallel devices with such a large V_{CC} difference until both on-resistances of power devices became equal. In the second experimental test, the static current imbalance is much lower compared to the first case and is attributed to the asymmetrical power circuit layout. As a result, the difference between the activation voltages (V_{CC}) of the power devices is much smaller compared to the V_{CC} difference of the first experimental test.

Lowering V_{CC} increases switching and conduction losses because the gate current decreases and on-resistance of SiC MOSFET increases. Therefore, it is important to suppress static current imbalance without increasing conduction losses. Static current imbalance can be minimized by equalizing the on-resistances either by increasing the on-resistance of the SiC MOSFET carrying the highest current or by reducing the on-resistance of the SiC MOSFET carrying the lowest current. However, the first static balancing approach will result in higher conduction losses compared to the second one. For this reason, in the first experimental test, the static current balancing process starts with the increase in V_{CC}, forcing the on-resistance of the SiC MOSFET with the least drain current to become lower. However, the absolute V_{CC} of the SiC MOSFET C2M0080120D is 25 V. As a result, the balancing process should be proceeded by decreasing the V_{CC} of the SiC MOSFET with the highest drain current until the on-resistances of both SiC MOSFETs become equal. The V_{CC} difference may influence dynamic current sharing, but it is compensated with the implementation of the proposed dynamic current balancing methods. As a result, the entire current imbalance is eliminated, retaining balanced switching and conduction power losses. Also, SiC MOSFETs operate under the same temperature stress level because distributed heat between power devices is kept almost equal. Since the drain-source voltage (V_{DS}) of both parallel devices is common, due to their parallel connection, and their drain currents become equal, switching and conduction power losses are balanced.

The turn-on current ringing is attributed to the free-wheeling SiC Schottky diode due to the discharge of its self-capacitance under reverse bias. On the other hand, the turn-off current ringing is caused by the parasitic inductance of the resistive load. The drain–source

voltage ringing during turn-off becomes lower with the use of the SiC Schottky diode but it cannot be dramatically reduced. Nevertheless, the switching oscillations of SiC MOSFETs could be eliminated with an RLC snubber [44]. However, the examination of the effectiveness of the proposed method is not affected by the current ringing during the switching intervals.

5. Design the Proposed Current Balancing Technique for Multiple-Device Operation

The scalability of current balancing techniques is very important since increased current capacity is required by medium- and high-power applications. For this reason, more than two SiC MOSFETs should be connected in parallel.

The proposed current balancing system is easy to implement for more than two parallel devices. The implementation design of the proposed method under the multi-device operation scenario is shown in Figure 19, considering N parallel-connected SiC MOSFETs. The extension of the proposed technique and adaption to the scenario with more than two parallel power switches requires one gate driver for every parallel power device. In addition, the algorithm should modify the control parameters for more than two power devices. Since each parallel device requires the generation of four PWM signals, the algorithm of the proposed method should be modified based on the number of parallel devices. Moreover, the number of parallel devices is defined by the number of FPGA switches for the control of the SiC MOSFETs and the adjustment of the balancing parameters of each device independently. Also, the maximum number of parallel SiC devices depends on the number of digital outputs of the constructed FPGA board.

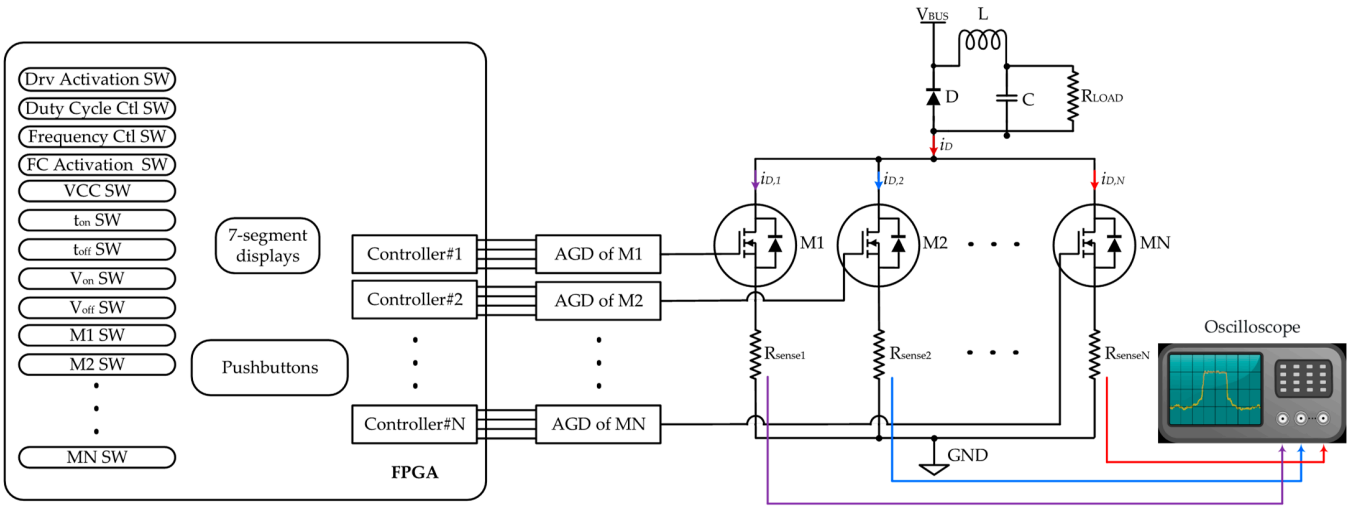


Figure 19. Implementation design of the proposed driving system for multi-device-parallel operation incorporated with a DC–DC buck converter.

6. Conclusions

In this paper, a novel autonomous open-loop current balancing technique for parallel-connected SiC MOSFETs is proposed. Regardless of the operating conditions, the proposed current balancing method can be realized without the need to know the deviation between the technical parameters to minimize current imbalance even if the PCB layout is asymmetrical. An active gate driver capable of manually modifying several control parameters with the help of an FPGA is proposed. As a result, the static current imbalance is eliminated by modifying the gate-source voltage of the proper power switch(es). Moreover, the dynamic current imbalance is suppressed by tuning the gate delays of the power devices through the adjustment of the turn-on delays and duty cycles of the driving pulses. The remaining dynamic imbalance is minimized through the variation in the gate currents. The current imbalance suppression ability of the open-loop technique is validated through experimental tests, demonstrating its performance and effectiveness against the main current imbalance

impact factors. The significance of the novel proposed method is huge in terms of efficiency and reliability for renewable energy sources and energy-saving systems.

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